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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,525	12/19/2000	Ebrahim Abedifard	400.063US01	6429

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FOGG SLIFER & POLGLAZE, P.A.
Attn: Thomas W. Leffert
P.O. Box 581009
Minneapolis, MN 55402

EXAMINER	
TRAN, THIEN F	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,525	ABEDIFARD, EBRAHIM	
	Examiner	Art Unit	
	Thien F Tran	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-65 is/are pending in the application.

4a) Of the above claim(s) See Continuation Sheet is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2,10-14,16-18,23-25,28,29,31-35,38,39,41-46,48,54,58,61,62,64 and 65 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Continuation of Disposition of Claims: Claims withdrawn from consideration are 3-9,15,19-22,26,27,30,36,37,40,47,49-53,55-57,59,60 and 63.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of claims in Paper No. 8 is acknowledged. The traversal is on the ground(s) that there are claims that are generic to multiple species. This is not found persuasive because it is well settled that species are required to be restricted if it is shown that these species are distinct. It is clearly established that species are in fact distinct in Paper No. 7.

The requirement is still deemed proper and is therefore made FINAL.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first semiconductor region enclosed in a second semiconductor region having the second conductivity type (the p-well enclosed in an n-well) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 10-14, 16-18, 23-25, 28-29, 31-35, 38, 39, 41-46, 48, 54, 58, 61-62 and 64-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (USPN 6,215,158) in view of Wang et al. (USPN 5,553,018).

Choi et al. disclose an n-channel memory device (Fig. 4) comprising: a first semiconductor region (upper well region 121) having a first conductivity type (p-type); a drain region 160 in the first semiconductor region, wherein the drain region has a second conductivity type (n-type) different from the first conductivity type; and a source region 140 in the first semiconductor region and having the second conductivity type; wherein the source region is coupled to a second semiconductor region (lower well region 130) underlying the first semiconductor region; and wherein the second semiconductor region has the second conductivity type. Choi et al. discloses a gate stack but does not explicitly disclose the memory device comprising a gate stack having a tunnel dielectric layer overlying the first semiconductor region; a floating-gate layer overlying the tunnel dielectric layer; an intergate dielectric layer overlying the floating-gate layer; a control-gate layer overlying the intergate dielectric layer. However, Choi et al. further discloses the memory device being a Flash memory device which inherently comprises a plurality of memory cells wherein each conventional memory cell is known to have a gate stack comprising a tunnel dielectric layer overlying the first semiconductor region; a floating-gate layer overlying the tunnel dielectric layer; an intergate dielectric layer overlying the floating-gate layer; a control-gate layer overlying the intergate dielectric layer as shown for example by Wang et al. Wang et al. discloses a Flash memory device comprising a gate stack having a tunnel dielectric layer 212

overlying the first semiconductor region; a floating-gate layer 214 overlying the tunnel dielectric layer; an intergate dielectric layer 216 overlying the floating-gate layer; a control-gate layer 218 overlying the intergate dielectric layer. Therefore, forming the memory cell of Choi comprising a conventional gate stack having a tunnel dielectric layer overlying the first semiconductor region; a floating-gate layer overlying the tunnel dielectric layer; an intergate dielectric layer overlying the floating-gate layer; a control-gate layer overlying the intergate dielectric layer would have been prima facie obvious.

Regarding claims 2, 18, the source region 140 is coupled to the second semiconductor region (lower well region 130) through a conductive source-line contact 231.

Regarding claims 10, 23, the source-line contact comprises a conductive fill material formed on sidewalls and a bottom of a contact hole and wherein the sidewalls of the contact hole are defined by the first semiconductor region (upper well region121) and the bottom of the contact hole is defined by an exposed portion of the second semiconductor region (lower well region130).

Regarding claims 11, 24, the source-line contact comprises a conductive material and wherein the conductive material includes one material of an implanted conductively-doped region having the second conductivity type (n-type).

Regarding claim 12, the first conductivity type is a p-type conductivity and the second conductivity type is an n-type conductivity.

Regarding claims 13, 44-46, the first semiconductor region is enclosed in a second semiconductor region having the second conductivity type.

Regarding claims 14 and 16, the floating-gate memory cell comprises a gate stack having a tunnel dielectric layer overlying an upper well region 121, wherein the upper well region has a first conductivity type; a floating-gate layer overlying the tunnel dielectric layer; an intergate dielectric layer overlying the floating-gate layer; a control-gate layer overlying the intergate dielectric layer; a drain region in the upper well region, wherein the drain region has a second conductivity type different from the first conductivity type; a source region 140 in the upper well region and having the second conductivity type, wherein the source region is coupled to a lower well region 130 ; and a source-line contact 231 extending from the source region to the lower well region 130; wherein the lower well region has the second conductivity type; and wherein the upper well region is formed in the lower well region.

Regarding claim 17, the tunnel dielectric layer is overlying and in contact with the upper well region 121, wherein the floating-gate layer is overlying and in contact with the tunnel dielectric layer, wherein the intergate dielectric layer is overlying and in contact with the floating-gate layer, and wherein the control-gate layer is overlying and in contact with the intergate dielectric layer.

Regarding claims 25, 31, 32 and 58, the memory device of Choi discloses a substrate 122 having a first conductivity type but does not explicitly disclose a plurality of word lines; a plurality of bit lines, a plurality of memory cells arranged in rows and columns with word lines coupled to rows of memory cells and bit lines coupled to columns of memory cells. It is conventional that a Flash memory device comprises a plurality of word lines, a plurality of bit lines, and plurality of memory cells arranged in

rows and columns with word lines coupled to rows of memory cells and bit lines coupled to columns of memory cell as shown for example by Wang et al. (see Fig, 2A), wherein a control gate layer is coupling to one of the plurality of word lines and a drain region is coupling to one of the plurality of bit lines. Therefore, forming the memory device of Choi comprising a plurality of word lines, a plurality of bit lines, a plurality of memory cells arranged in rows and columns with word lines coupled to rows of memory cells and bit lines coupled to columns of memory cells, wherein a control gate layer is coupling to one of the plurality of word lines and a drain region is coupling to one of the plurality of bit lines would have been prima facie obvious.

Regarding claims 28, 29, 38, 39, 48, 61, 62, each source-line contact extends through only one source region.

Regarding claims 33, 34, region 121 is considered as a first well region; a second well region and a fourth well region are the same well region 130; a third well region and the substrate are the same region 122. The array of memory cells in Choi is considered as having two blocks of memory cells.

Regarding claim 35, each control-gate layer coupled to each word line of the first plurality of word lines is associated with a floating gate memory cell of the first block of floating-gate memory cells.

Regarding claims 41, 42, region 121 is the well region and region 130 is the interposing well region.

Regarding claim 43, Choi further discloses the use of p-channel devices employing an n-tub (col. 3, lines 30-34). Therefore, the well region 121 having the first

conductivity type is also an n-well and the interposing well region 130 having the second conductivity type is a p-well in an n-type semiconductor substrate.

Regarding claims 64 and 65, Choi does not discloses the memory device being used in an electronic system comprising a processor. However, it is well known that an electronic system, for example, a computer comprises a processor, a memory device and a plurality of data lines coupled between the array of memory cells and the processor. It would have been obvious to form the memory device of Choi as a part of the computer for the advantages that Choi provides.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F Tran whose telephone number is (703) 308-4108. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

tt
February 21, 2003

Thien Tran
Patent Examiner
Technology Center 2800